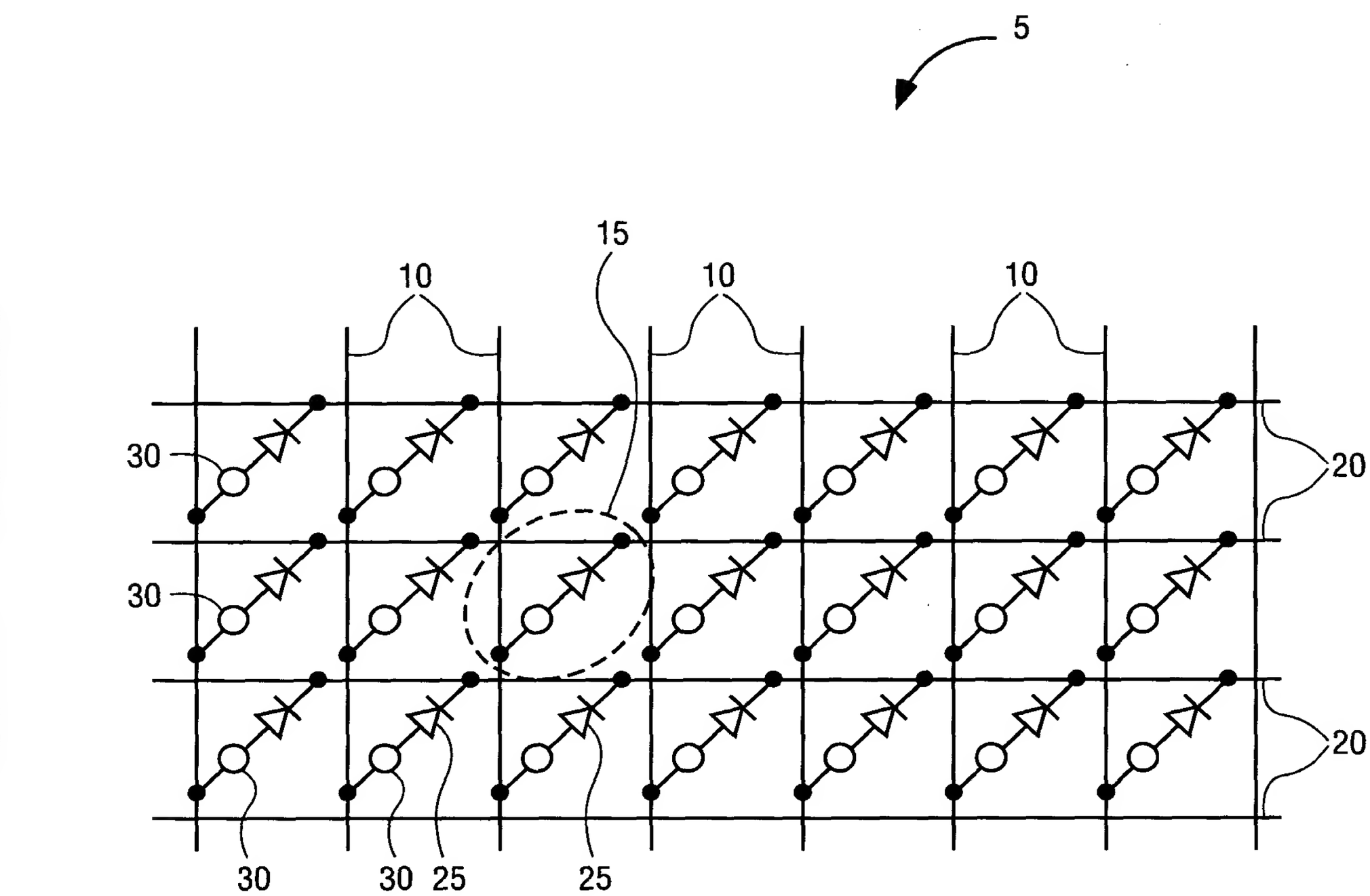


FIG. 1

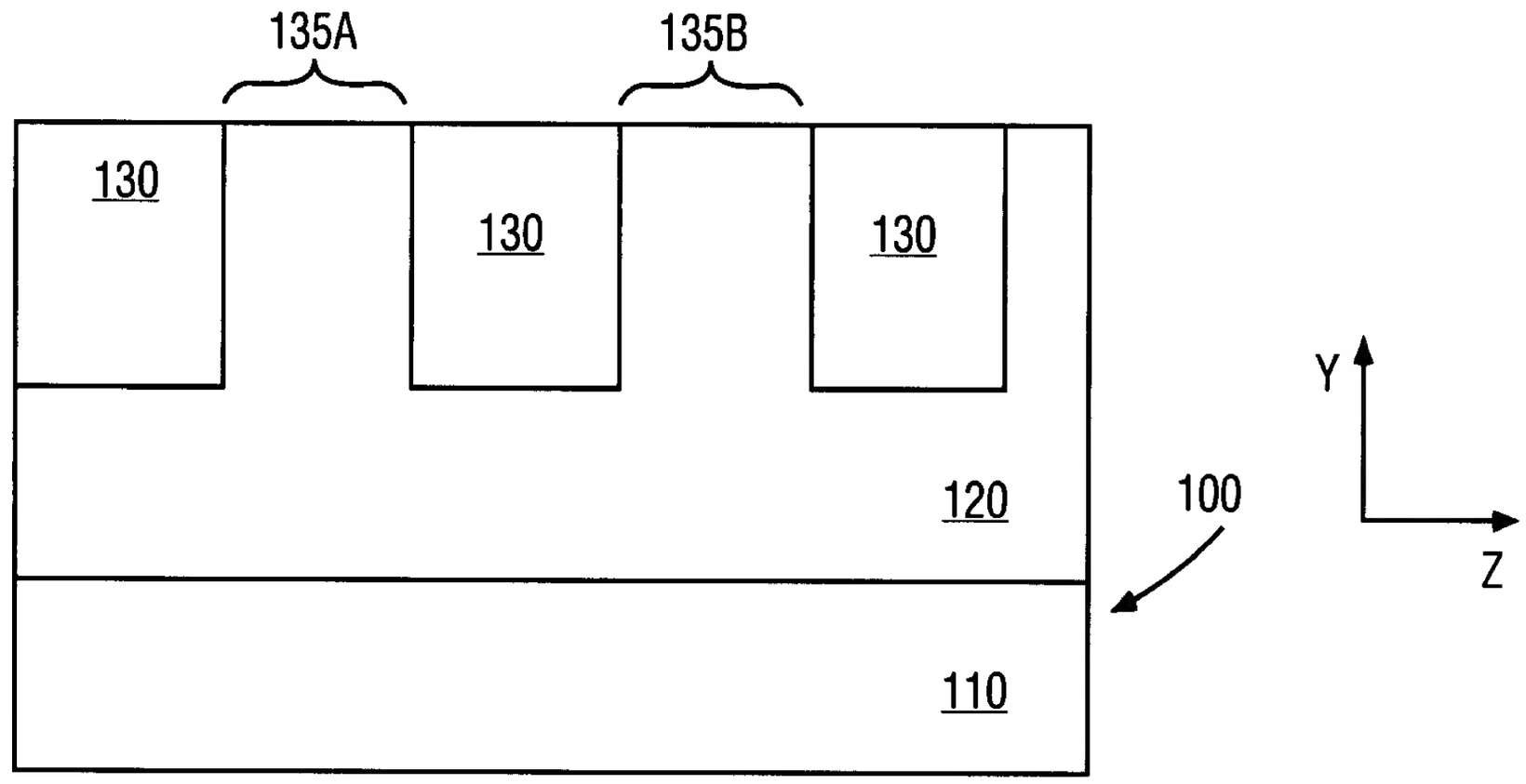


FIG. 2

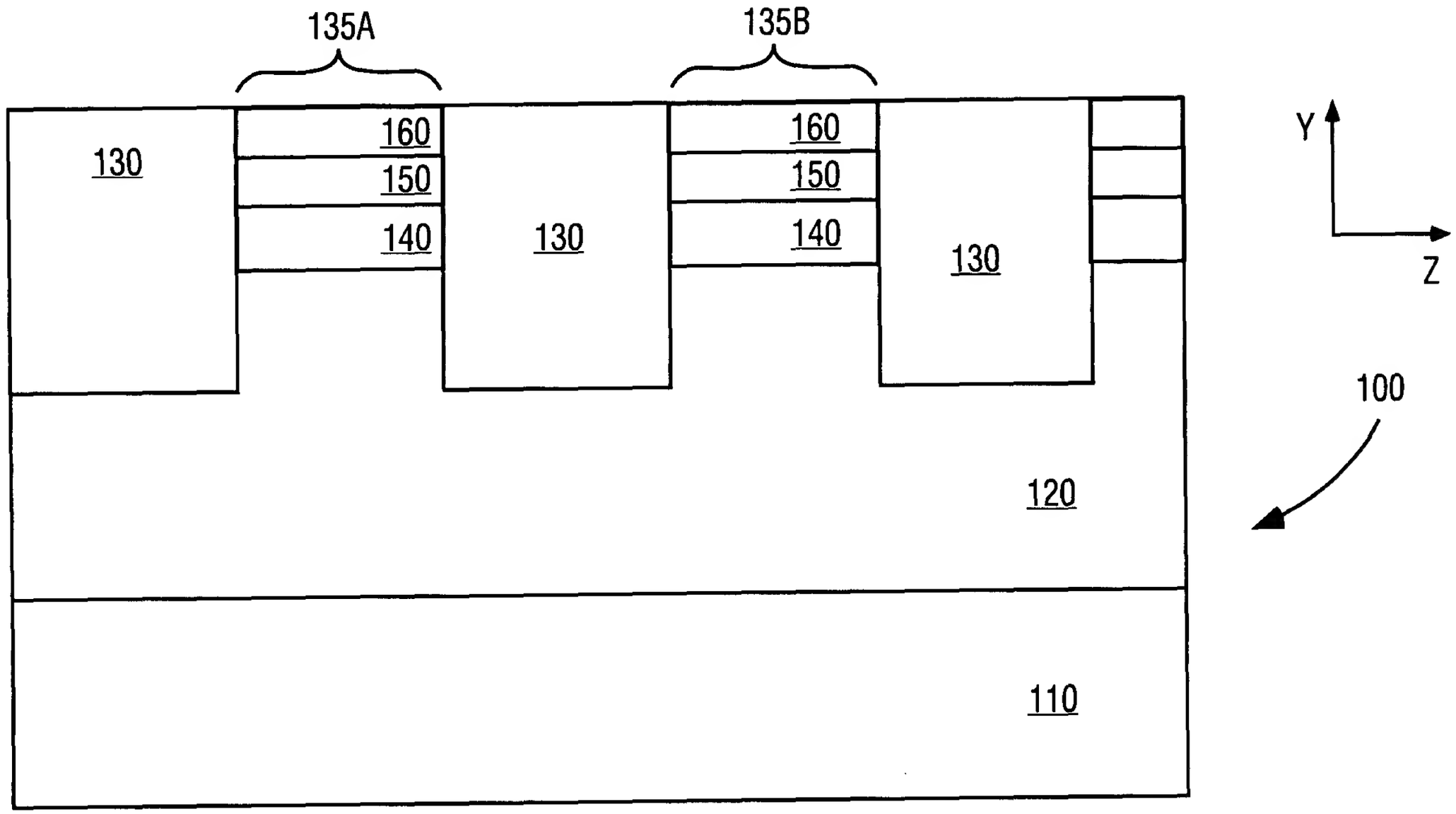


FIG. 3

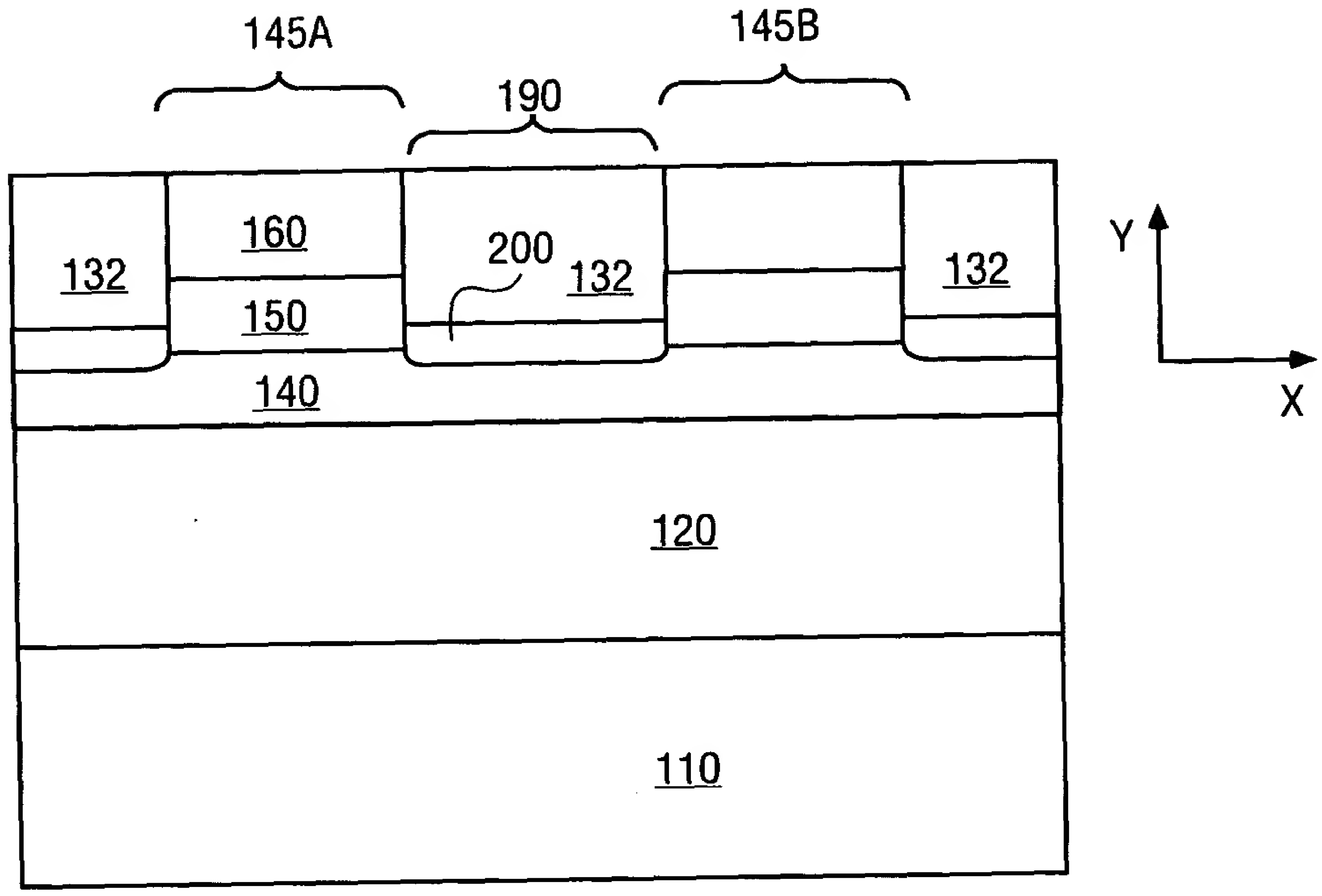

145A
190
145B
160
132
200
132
132
150
140
120
110
Y
X

FIG. 4

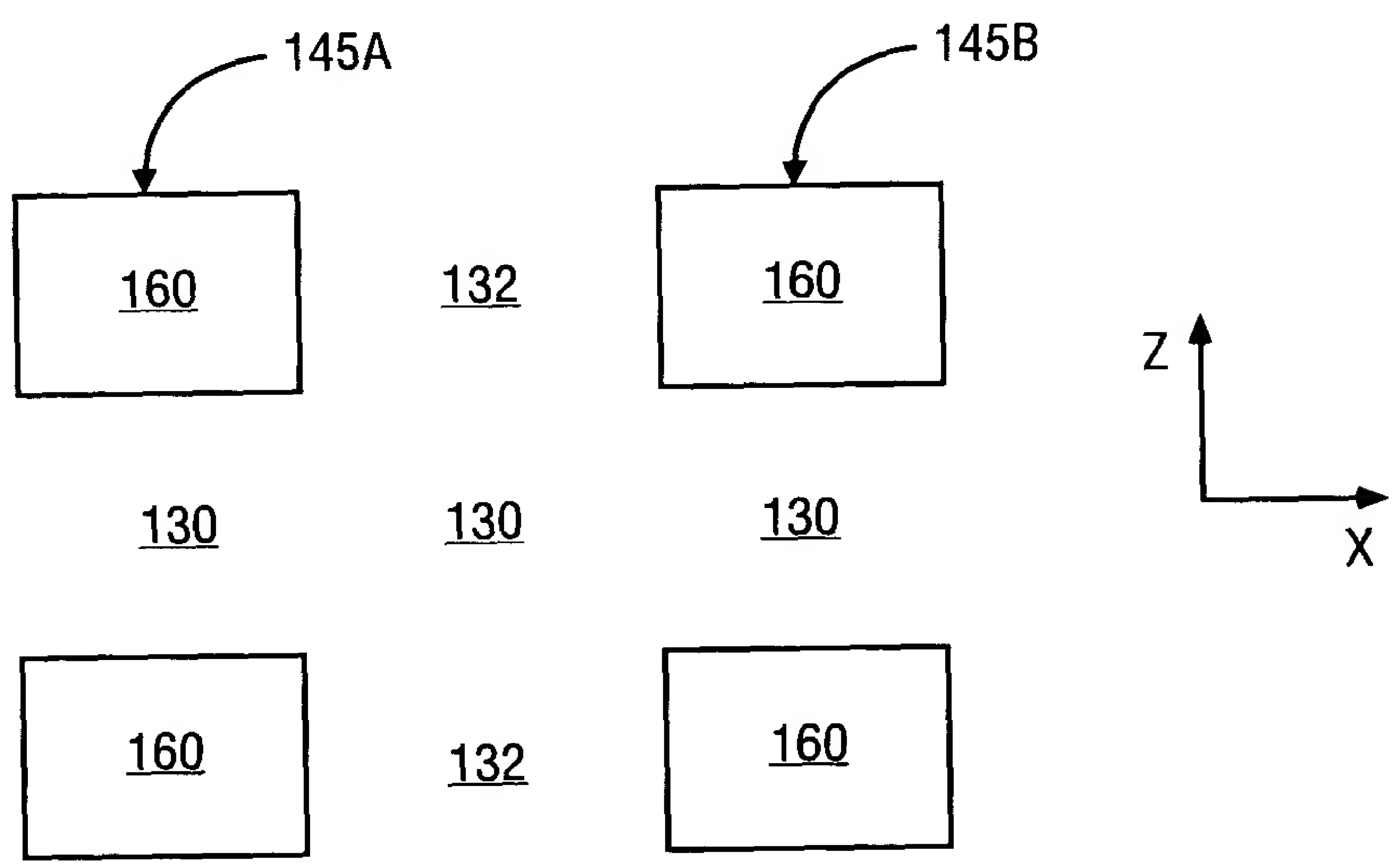

145A
145B
160
132
160
Z
130
130
130
X
160
132
160

FIG. 5

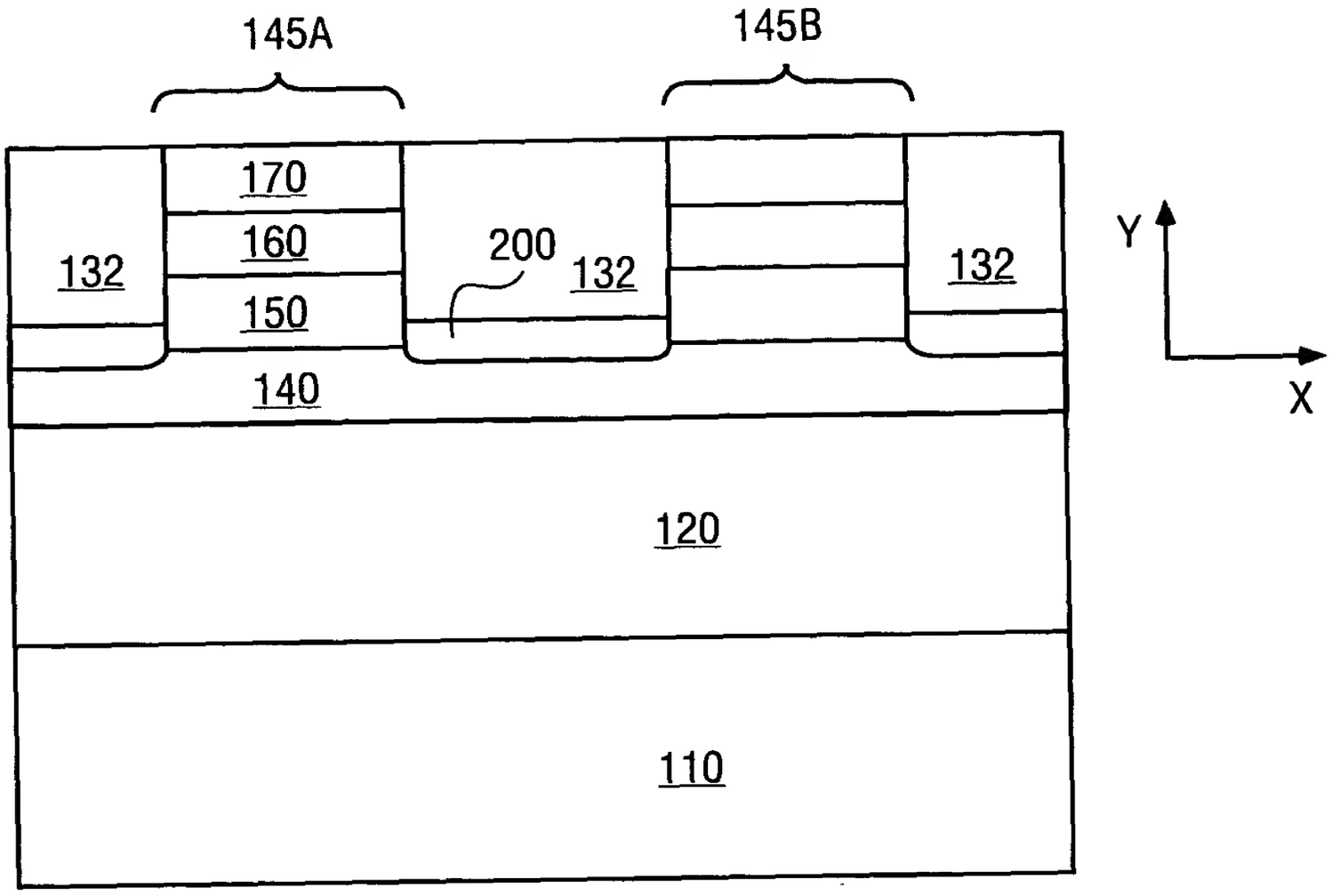

145A
145B
170
160
150
132
200
132
132
140
120
110
Y
X

FIG. 6

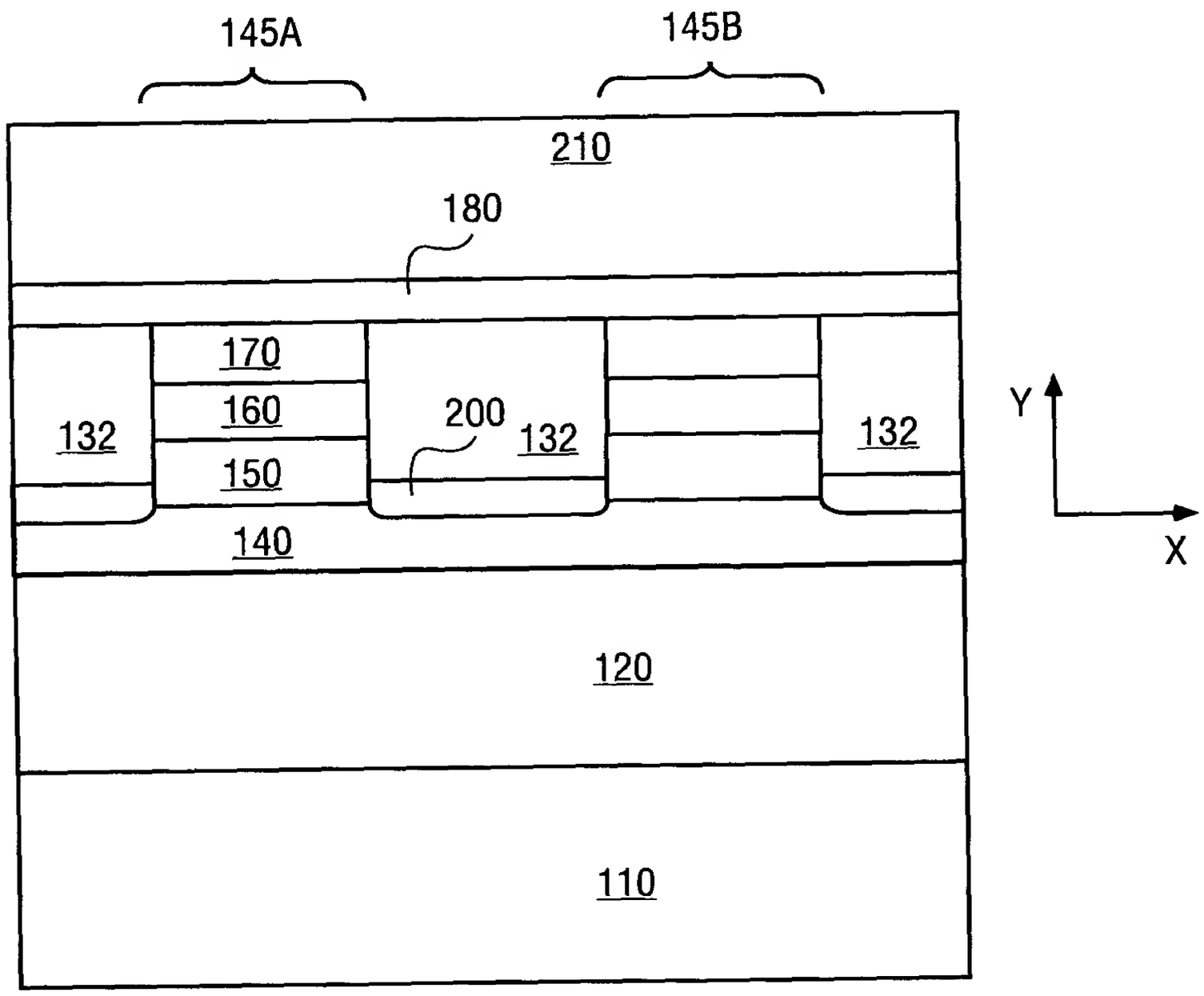

145A
145B
210
180
170
160
150
132
200
132
132
140
120
110
Y
X

FIG. 7

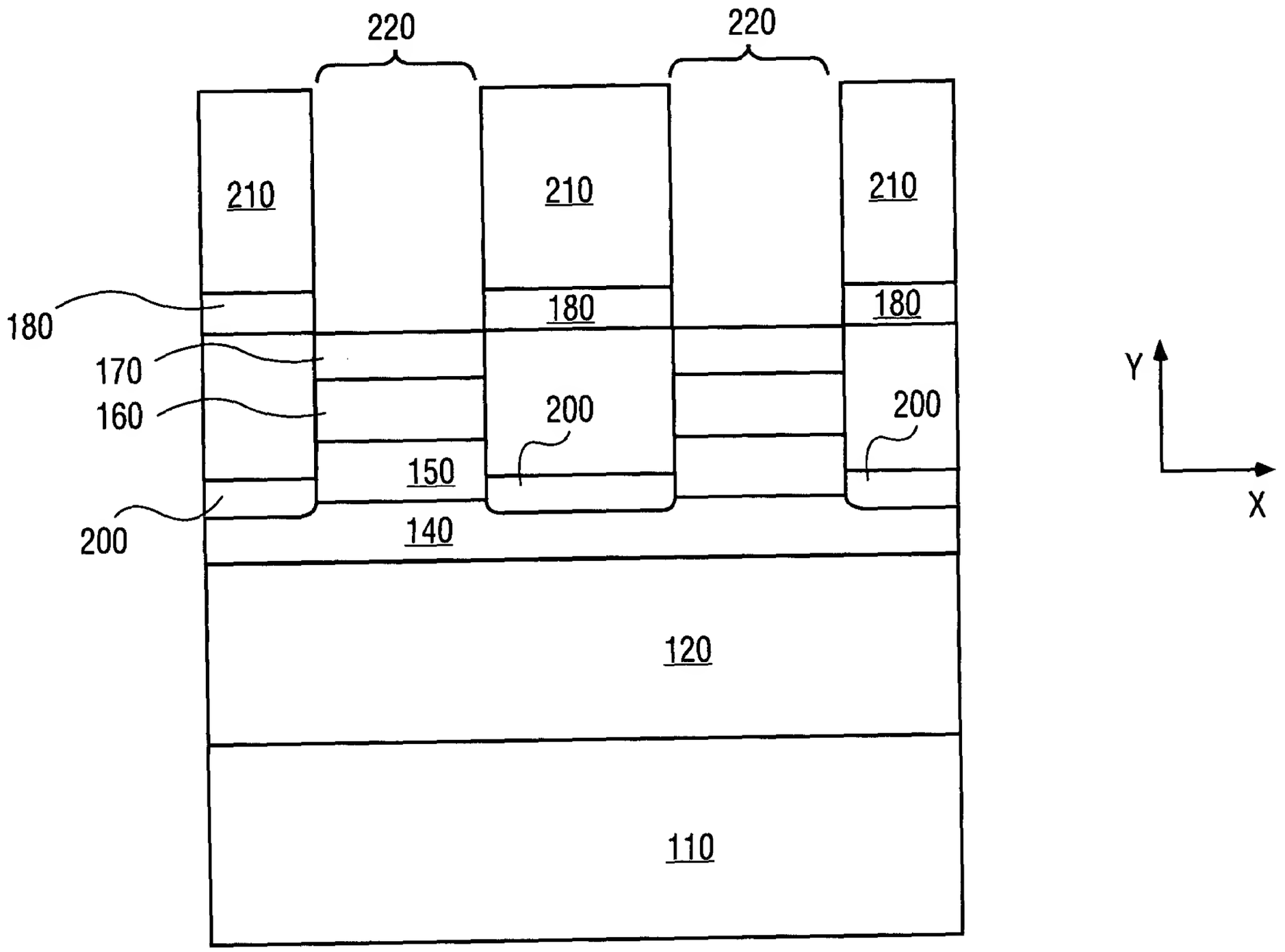

220
220
210
210
210
180
180
180
170
160
200
200
150
200
140
120
110
Y
X

FIG. 8

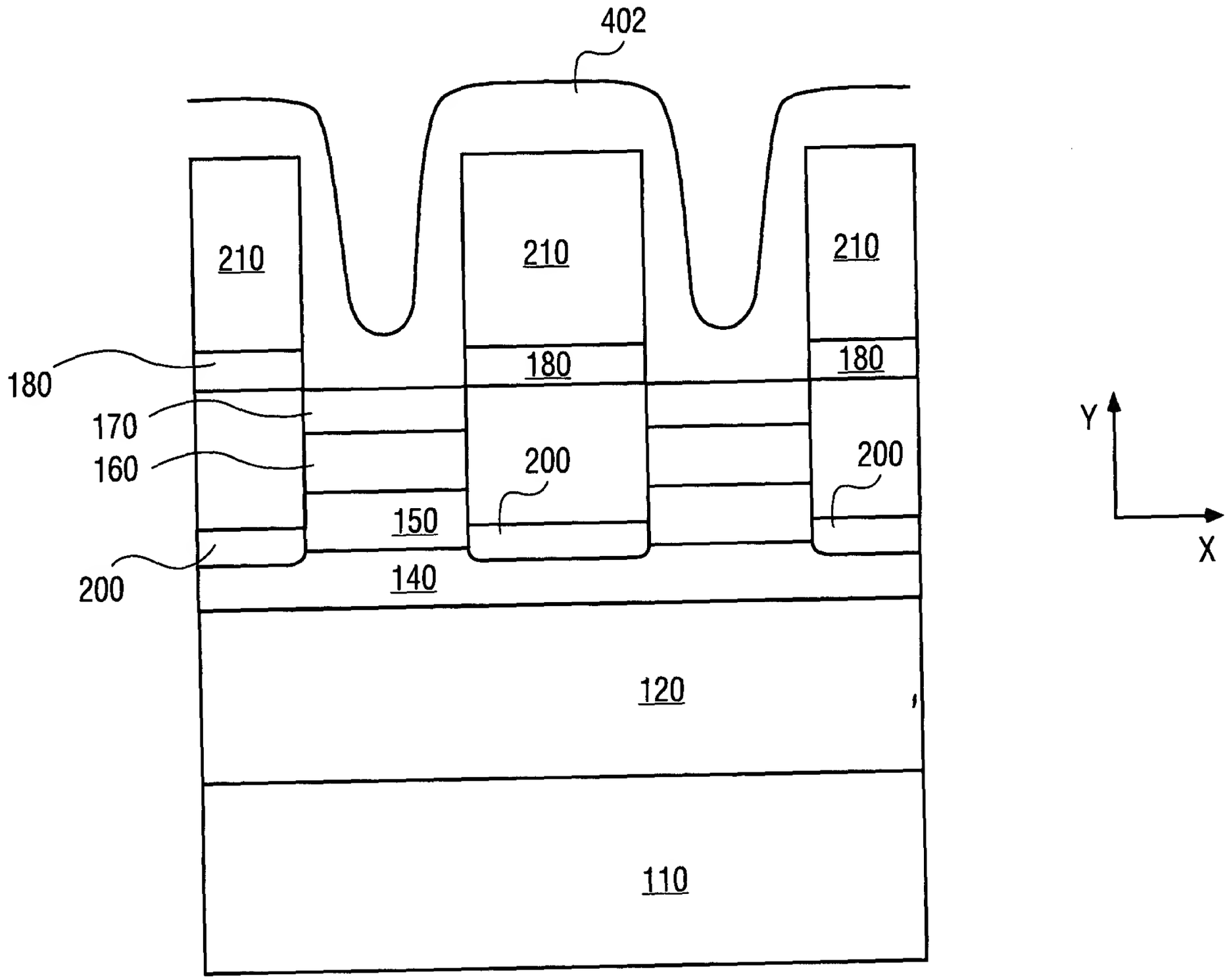

402
210
210
210
180
180
180
170
160
200
200
150
200
140
120
110
Y
X

FIG. 9

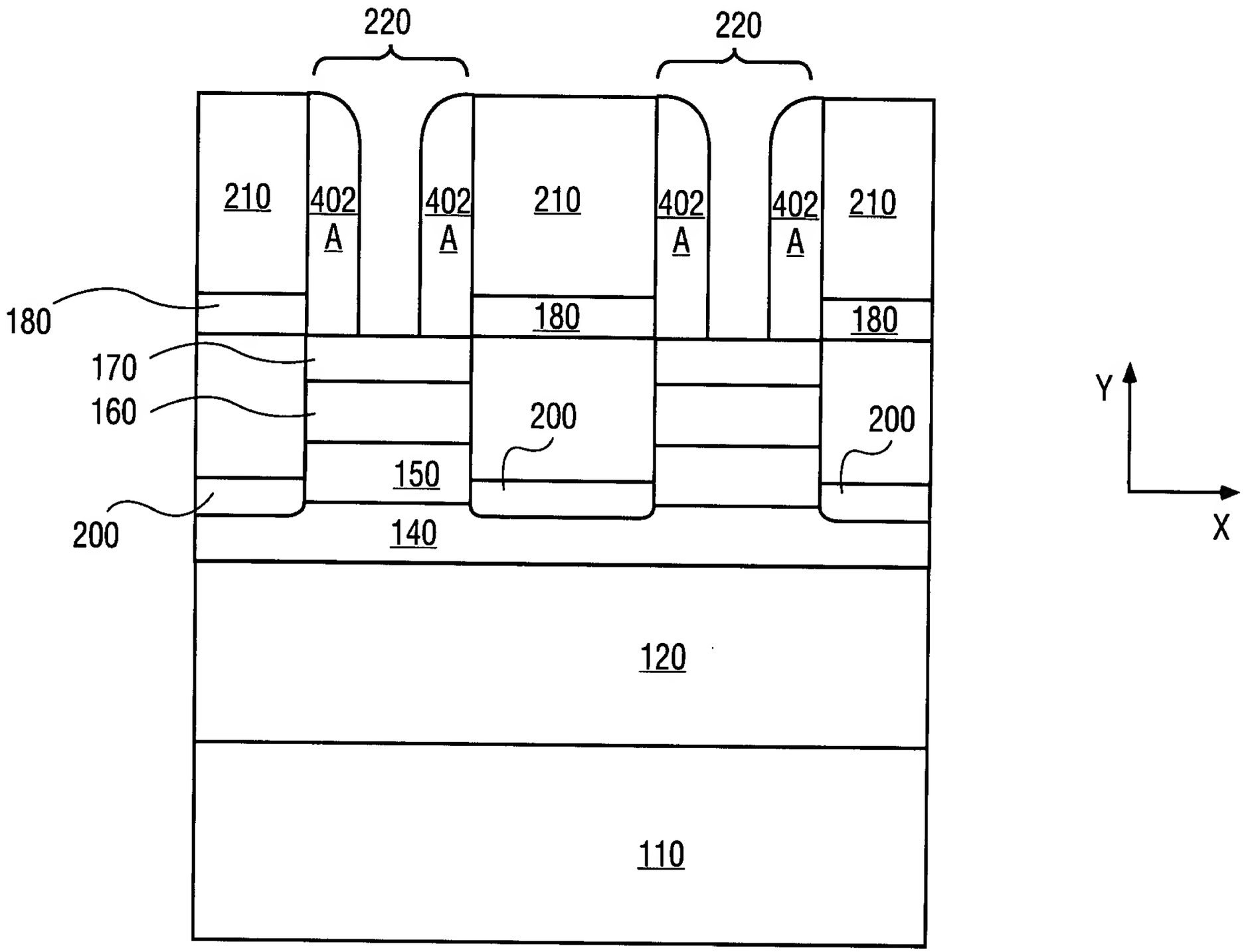

220
220
210
402 A
402 A
210
402 A
402 A
210
180
180
180
170
160
200
200
150
200
140
120
110
Y
X

FIG. 10

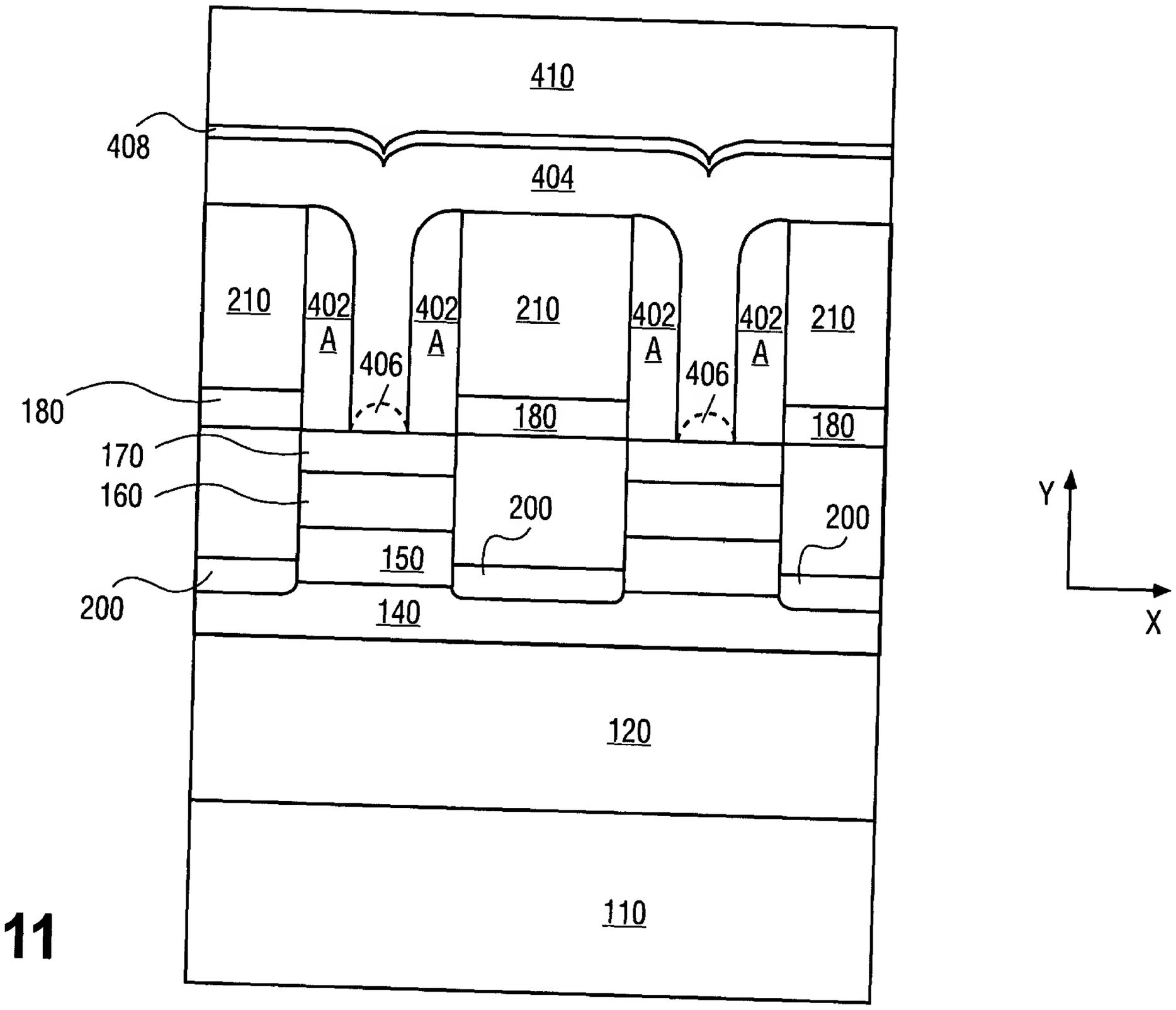


FIG. 11

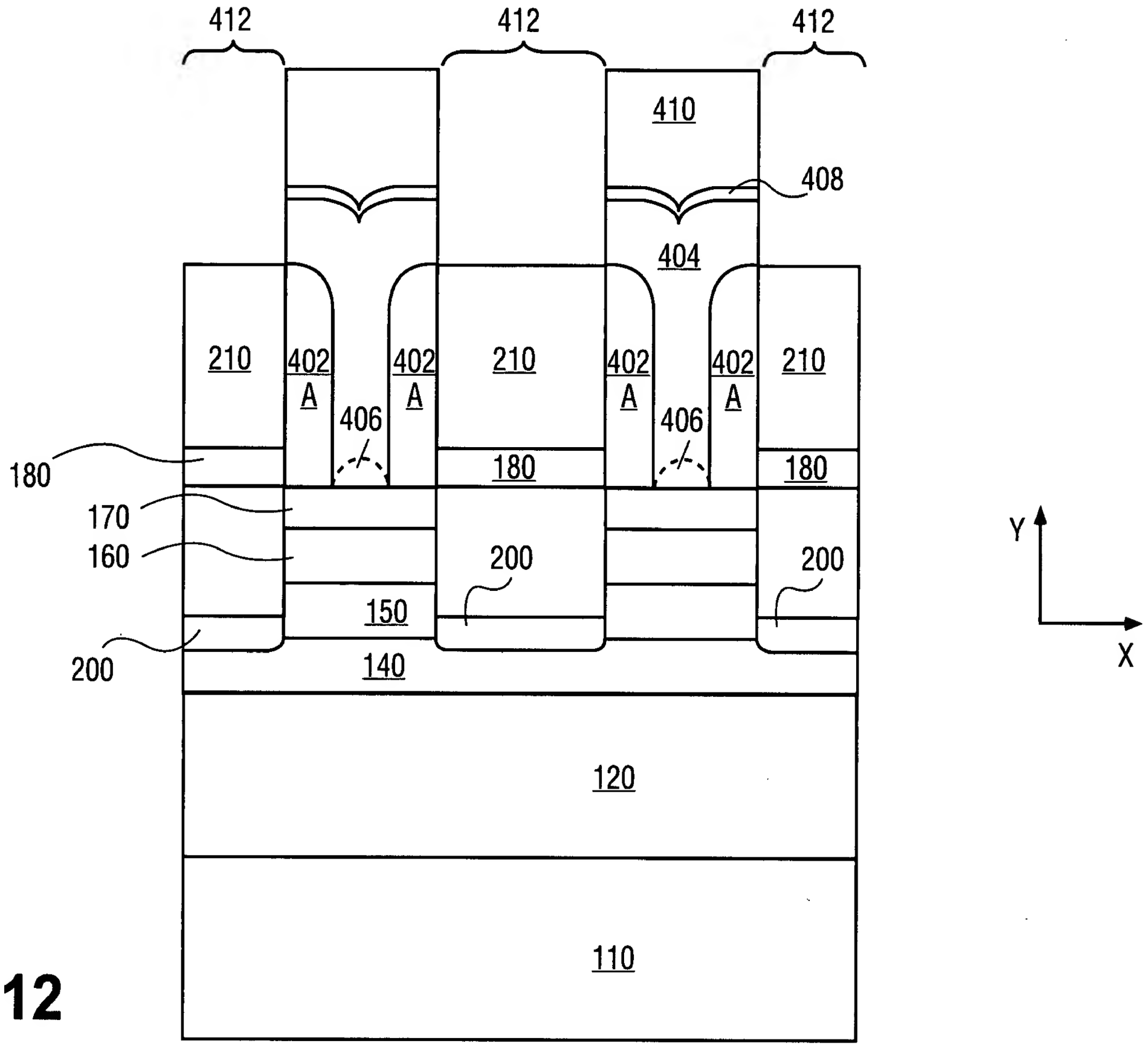

412
412
412
410
408
404
210
402 A
402 A
210
402 A
402 A
210
406
406
180
180
180
170
160
200
200
200
150
140
120
110
Y
X

FIG. 12

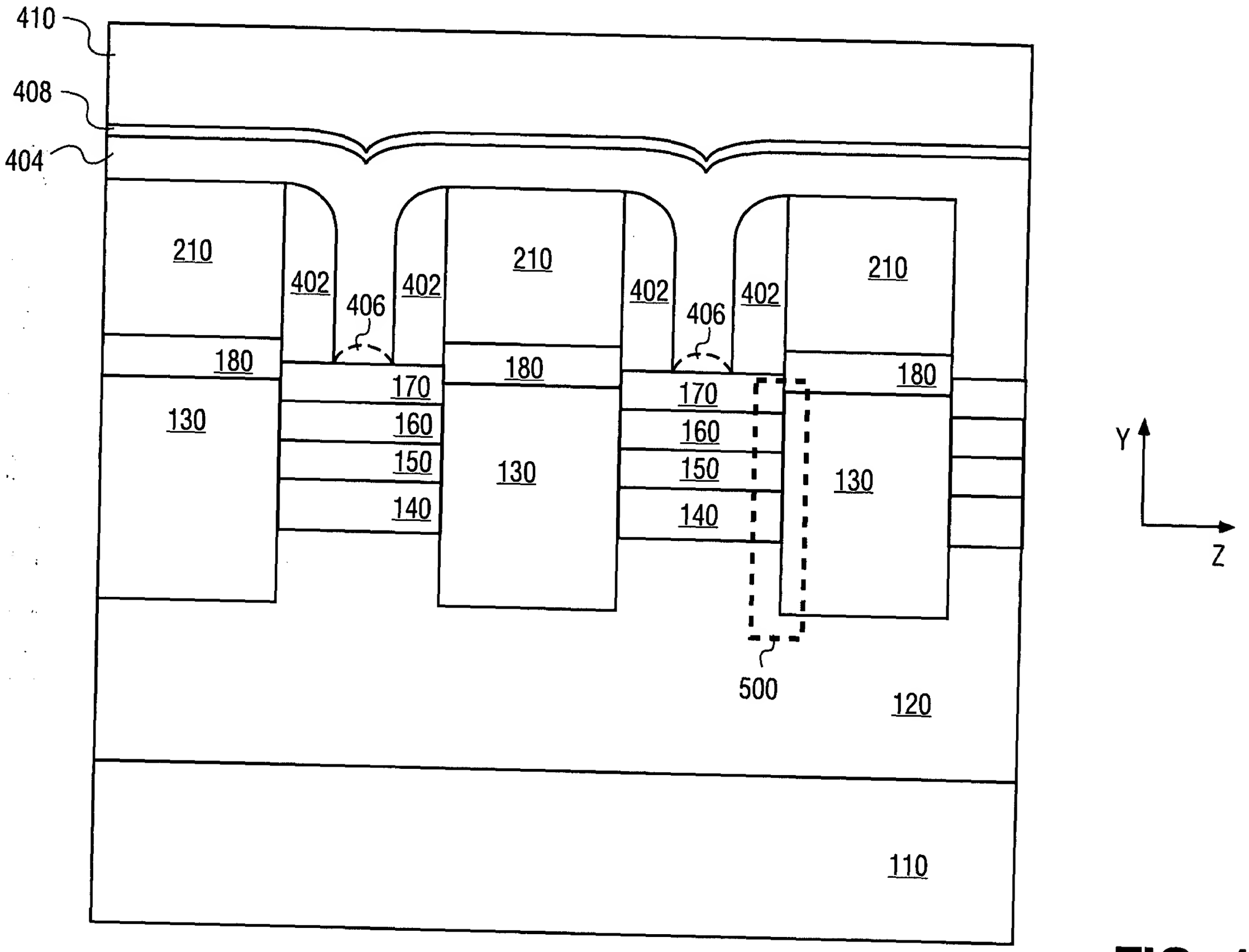
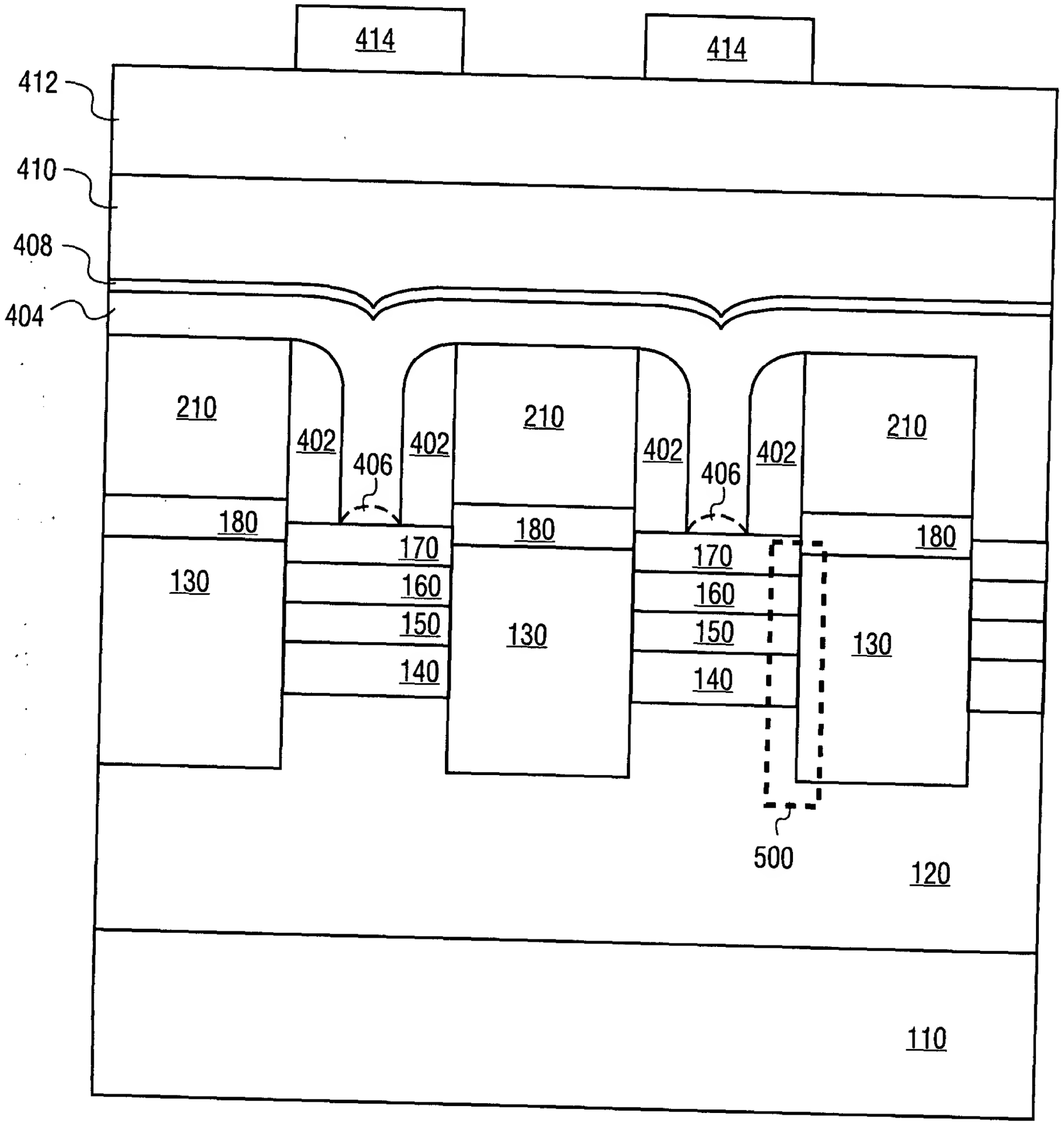

410
408
404
210
402
406
402
210
402
406
402
210
180
180
180
170
170
160
160
150
150
140
140
130
130
130
500
120
110
Y
Z

FIG. 13


414
414
412
410
408
404
210
210
210
402
402
402
402
406
406
180
180
180
170
160
150
140
170
160
150
140
130
130
130
500
120
110

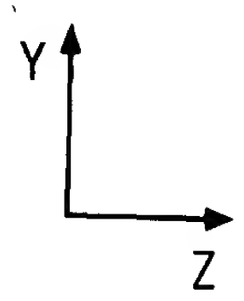

Y
Z

FIG. 14

FORM A DIELECTRIC ON A CONTACT, THE CONTACT FORMED ON SUBSTRATE.

↓

FORM AN OPENING THROUGH THE DIELECTRIC EXPOSING THE CONTACT.

↓

OPTIONALLY, FORM A SPACER WITHIN THE OPENING AND OPTIONALLY CONFORMALLY FORM THE SPACER ON THE DIELECTRIC AND WITHIN THE OPENING; AND FURTHER OPTIONALLY ANISOTROPICALLY ETCH THE SPACER FROM THE DIELECTRIC USING AN AGENT SELECTIVE FOR THE SPACER.

↓

FORM PROGRAMMABLE MATERIAL WITHIN THE OPENING, THE PROGRAMMABLE MATERIAL ON THE CONTACT.

↓

FORM A CONDUCTOR TO THE PROGRAMMABLE MATERIAL.

↓

OPTIONALLY, FORM A BARRIER BETWEEN THE PROGRAMMABLE MATERIAL AND THE CONDUCTOR.

↓

OPTIONALLY, FORM AN ISOLATION DEVICE BETWEEN THE CONTACT AND A SIGNAL LINE.

↓

FORM A DIELECTRIC ON THE CONDUCTOR.

↓

FORM A VIA IN THE DIELECTRIC TO THE CONTACT. FILL THE VIA WITH CONDUCTIVE MATERIAL.

↓

FORM A CONDUCTOR ON THE DIELECTRIC.

FIG. 15

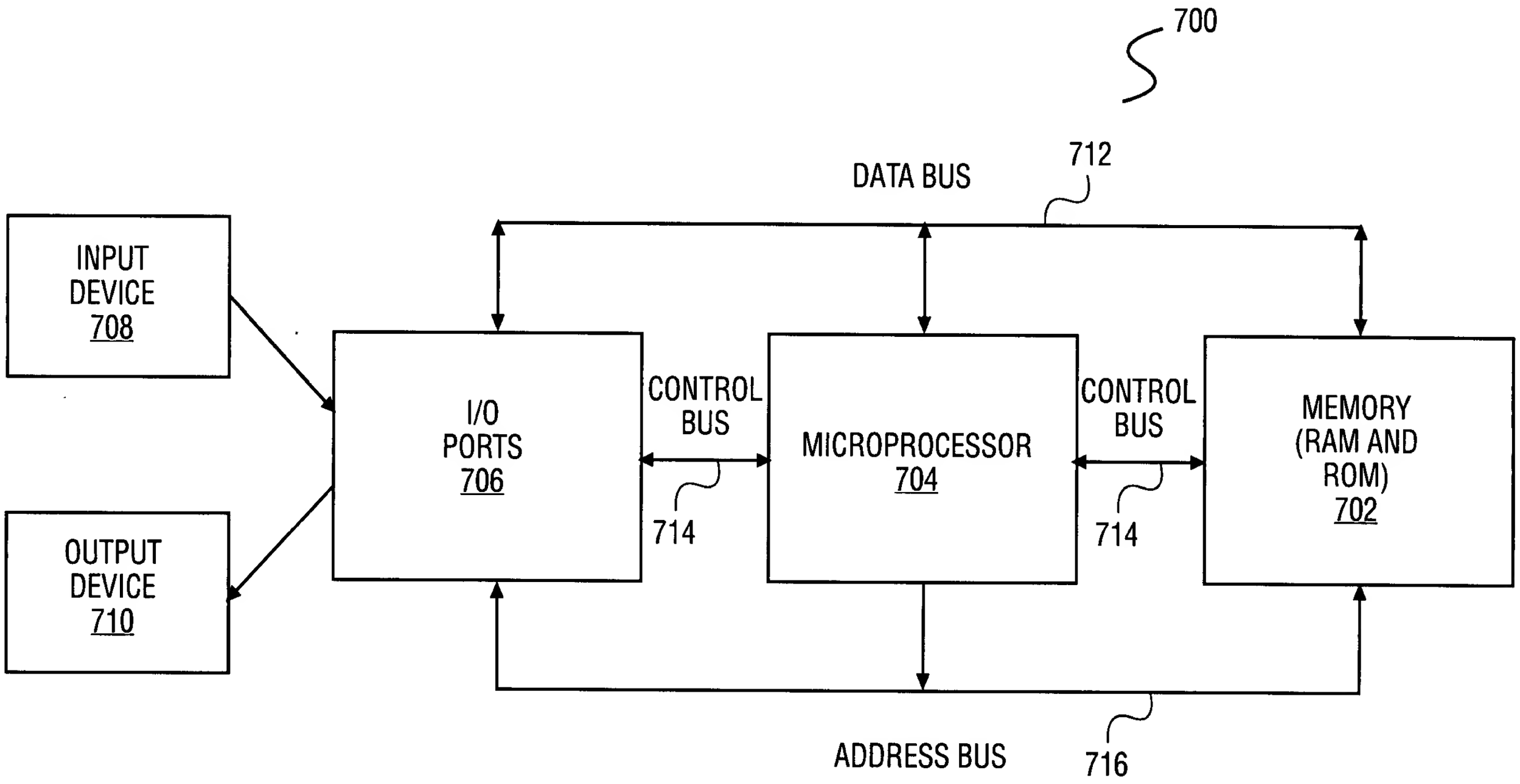

700
DATA BUS
712
INPUT DEVICE 708
OUTPUT DEVICE 710
I/O PORTS 706
CONTROL BUS
714
MICROPROCESSOR 704
CONTROL BUS
714
MEMORY (RAM AND ROM) 702
ADDRESS BUS
716

FIG. 16